P27157.D01 Serial No.: 10/689,506

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Haujie CHEN, *et al.*

Docket No. P27157

Confirmation No. 4303

Group Art Unit: 2813

Appln. No. : 10/689,506

Examiner: N. O. Berezny

Filed : October 20, 2003

For : HIGH PERFORMANCE STRESS-ENHANCED MOSFETs USING Si:C AND SiGe EPITAXIAL SOURCE/DRAIN AND METHOD OF MANUFACTURE

DECLARATION UNDER 37 C.F.R. 1.131

Sir:

We, Huajie Chen, Dureseti Chidambarrao, and Omer H. Dokumaci do hereby declare:

We are co-inventors of the subject matter disclosed and recited in independent claims 1 and 10 of the above-identified application.

2. We completed the invention of claims 1 and 10 (and those claims dependent thereon) in the United States before June 17, 2003, as evidenced below.

CONCEPTION

3. Before June 17, 2003, we conceived of a method of manufacturing a semiconductor structure, comprising the steps of forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate, forming a pFET stack in the pFET channel and an nFET stack in the nFET channel, providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel and

providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel before June 17, 2003.

4. We also conceived of a method of manufacturing a semiconductor structure, comprising the steps of forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate, forming a pFET structure and an nFET structure on the substrate associated with the pFET channel and the nFET channel, respectively, etching regions of the pFET structure and the nFET structure, forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel, forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel, and doping source and drain regions of the nFET and pFET structures.

5. Evidence of such conceptions as disclosed and recited in claims 1 and 10 of the application is shown in an embodiment of which is evidenced by IBM Invention Disclosure BUR8- 0318 (hereinafter referred to as "the Invention Disclosure") attached hereto as Exhibit A. The Invention Disclosure attached hereto is a photocopy of and are identical to the originals, except that all pertinent dates have been removed therefrom.

6. All relevant dates removed from the Invention Disclosure and other attached documents attached hereto are before June 17, 2003.

7. The benefits and features of the recited invention are shown and described in the Invention Disclosure and accompanying documents.

8. These features and others are exemplified in the figures accompanying the Invention Disclosure.

DUE DILIGENCE

9. At least inventor Dureseti Chidambarrao communicated with outside patent counsel, Andrew M. Calderon, in preparing a patent application based on the Invention Disclosure.

10. We worked diligently on the preparation of the patent application by first submitting the Invention Disclosure statement to in-house IBM counsel on June 9, 2003.

11. After a prior art search was conducted and the Invention Disclosure was mailed to outside counsel, Andrew M. Calderon, we worked diligently on the preparation of the patent application with outside patent counsel Andrew M. Calderon until a final draft patent application was completed to our satisfaction. Communications took place between at least one of the inventors and Mr. Calderon on at least August 26, 2003, September 20, 2003 and October 13, 2003.

12. A final draft of the patent application was forwarded to inventor Dureseti Chidambarrao on October 13, 2003 for execution of the formal documents by all of the inventors. The inventors signed the documents for filing in the U.S. Patent and Trademark Office, which was effectuated on October 20, 2003 by outside counsel.

13. We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Huajie Chen	Date
Dureseti Chidambarrao	Date
Omer H. Dokumaci	08/16/2005 Date